

Abstract

In this note we want to summarize the setup, the resources and manpower available in our laboratory in BNL and what we believe should be upgraded in order to run at BNL system tests on the front-electronics of the Atlas Liquid Argon (LARG) calorimeter.

Introduction

Production of the ATLAS Liquid Argon calorimeter (LARG) front-end (FE) electronics boards that will be installed on the custom Front-End Crate (FEC) is approaching. The need of system tests that will validate the design of all the boards in an environment close to the final experiment one has been foreseen by the LARG FE steering group. A task force has been formed to decide over what tests to be performed, in what configuration and where to do such tests.

The purpose of this document is to present BNL facilities and expertises that can be used to accomplish the crate-tests in the time-framework dictated by the production of the boards (e.g. the PRR of the FEBs has been foreseen in Dec. 2002). This document will limit its scope in a description of what resources are currently available and what upgrades are currently planned for the completion of the setup and/or in view of such tests.

It is based on the following generic assumptions:

1. The final tests will be eventually done at CERN on the real detector during the detector commissioning. However for practical reasons it was suggested to perform initial studies and tests at an alternative site, profiting from the availability of already existing resources and infrastructures and from the possibility to have dedicated manpower for long periods (≥ 4 months).
2. The experience and the results of such preliminary tests should result in the definition of system procedures that can be proposed as standards. In this respect all the tests, tools and expertises that will be developed at the test-site have to be easily transferable to CERN and to the entire LARG community so that can be used during the installation and commissioning of the detector.
3. The setup has to reproduce as close as possible the conditions that likely will be present in the real experiment.
4. Tests should be focused on the system and architectural aspects of the front-end electronics readout. In particular here matters how the whole system affects the behaviour of the boards and limits its performance (e.g. coherent noise or EMI studies on the FEBs, signal routing to the TB boards, crosstalk...). Performances of the single board will be evaluated in the laboratories responsible for the board design and production.
5. A large fraction of a FEC has to be operationally working and read-out (not less than half a crate). The requirements should derive from physics considerations (high energy τ -jets and E_T^{miss} reconstruction for example are usually done with $\Delta R \simeq 0.7$, which is approximately half-crate for the EM barrel) and it's a responsibility of the task-force to define exactly how many boards and what configuration should be used.

The setup

Fig. 1 is a block diagram of the mockup/teststand available in BNL for running the crate-tests. The diagram shows the main subsystems that define the current setup:

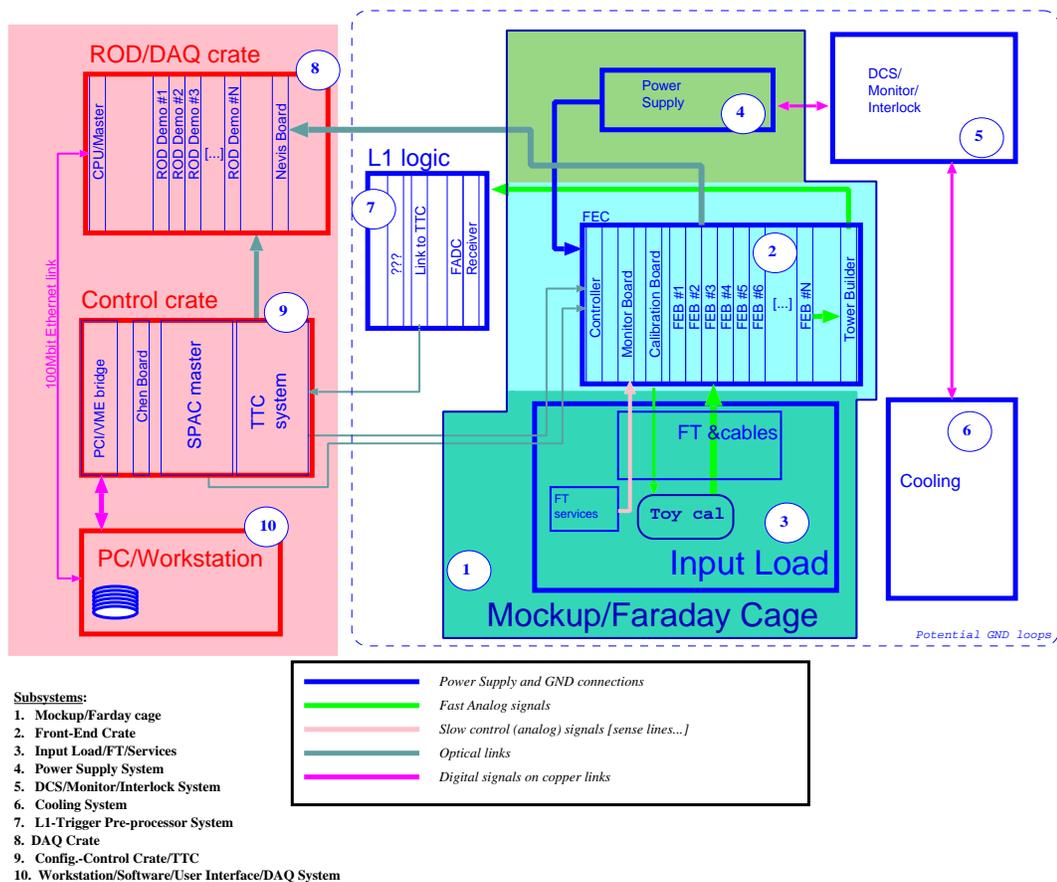


Figure 1: Block diagram of the BNL setup for full-crate tests

1. Mockup/Mechanical Infrastructure/Faraday Cage
2. Front-End Crate
3. Input Load/Services
4. Power Supply
5. Monitor/Interlock/DCS
6. Cooling
7. L1/sum analyzer system
8. ROD/DAQ crate
9. Control and configuration
10. Workstation/Software/User Interface/DAQ system

1 Mockup

The existing mockup is a full scale mixed wood+stainless steel+aluminum structure shown in Fig. 2. It represents 1/16 of the barrel cryostat made of an aluminum mechanical support that allows rotations in φ . Tilecal walls and fingers, cooling manifolds and 2 FEC prototypes are visible in the picture. An early power supply module prototype (also shown in the picture) has been installed between the tilecal fingers and connected to the left-side FEC.

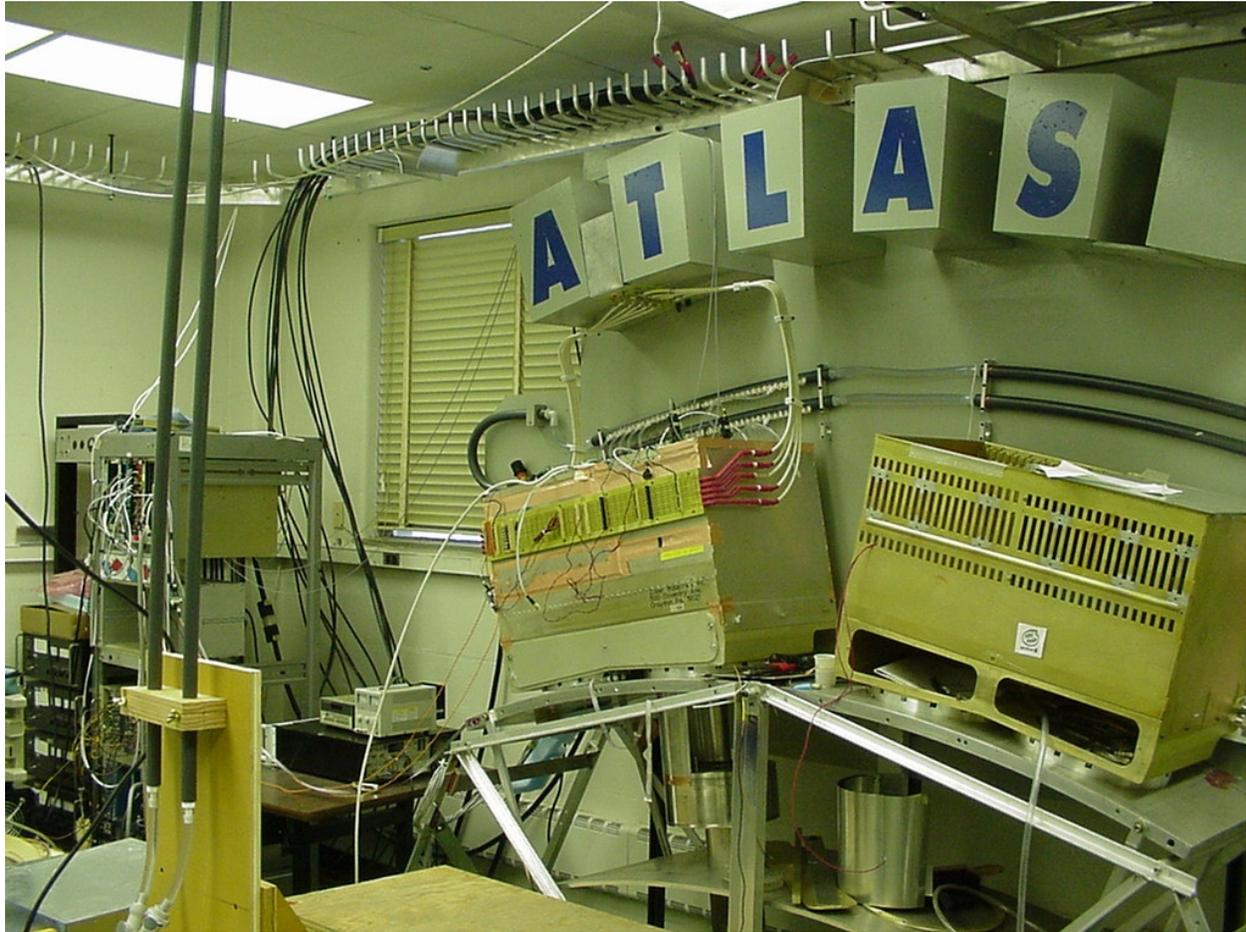


Figure 2: Picture of the present mockup

We propose and we plan to complete the setup for the crate tests as follows:

i) integration of a production vacuum feedthrough (FT) in the mockup

BNL is producing 68 FTs (64 for installation + 4 spares). We agreed that 2 FTs will be for the duration of the tests on our setup.

ii) enclosure completion.

The mechanical support will be enclosed in an aluminum structure that will house the input loads, simulating the cryostat walls and therefore realizing a Faraday cage as in the real detector (conforming to the ATLAS/LARG grounding policy).

iii) manifold replacement.

Cooling manifolds will be replaced to accommodate for the final insertion fitting (see Sec. 6)

Table 1 summarizes the actions needed and the schedule foreseen:

Table 1: actions and schedule for mockup upgrade

Action	Responsability	Start Date	Duration
Manifold replacement	BNL	04/14/02	1d
FT integration	BNL	04/15/02	10d
Enclosure	BNL		
Design		04/01/02	20d
Installation		05/01/02	20d

2 Front-End Crate

Fig. 3 shows a block diagram of the front-end crate (FEC). It shows all the components that have to be installed in it.

An ID tag has been assigned to the crate subsystem (as well as to all the others) for convenience only. White boxes represent components BNL is directly responsible for, while responsibility for components in green boxes belong to other institutions.

Table 2 summarizes the status of the components BNL is responsible for. In addition an approximate schedule with few intermediate steps is also presented. Notice that for each part the quantity is depending on the configuration of the crate tests. However is clear that most commercial parts are included in a larger purchase order for the full ATLAS production which takes into account spares etc.

Notice that items 2.1 to 2.7 will be produced, delivered and installed in BNL. Items 2.8.1 and 2.8.2 once delivered will be stored in BNL until the boards from other institutions will be made available for their installation. On the other end items 2.8.3 to 2.8.8 has to be delivered to the institutions for board assembling. A deadline for such delivery and the exact quantity has to be specified by the institution responsible for the board production.

Item 2.8.2 is potentially on the critical path. In particular the production of the Aluminum contacts that interface the board components to the cooling plates may be a concern. It's desirable that institutions responsible for the board production could provide us with 3D-maps of the boards (i.e. with component heights specified). This would allow for the design of such contacts in advance. Alternatively, as soon as the first assembled boards are available, a sample could be sent to BNL for measurements. The scenario we want to avoid is to design and manufacture (in house) such contacts only when the boards are shipped to BNL for the crate-tests (which presumably will be not before September).

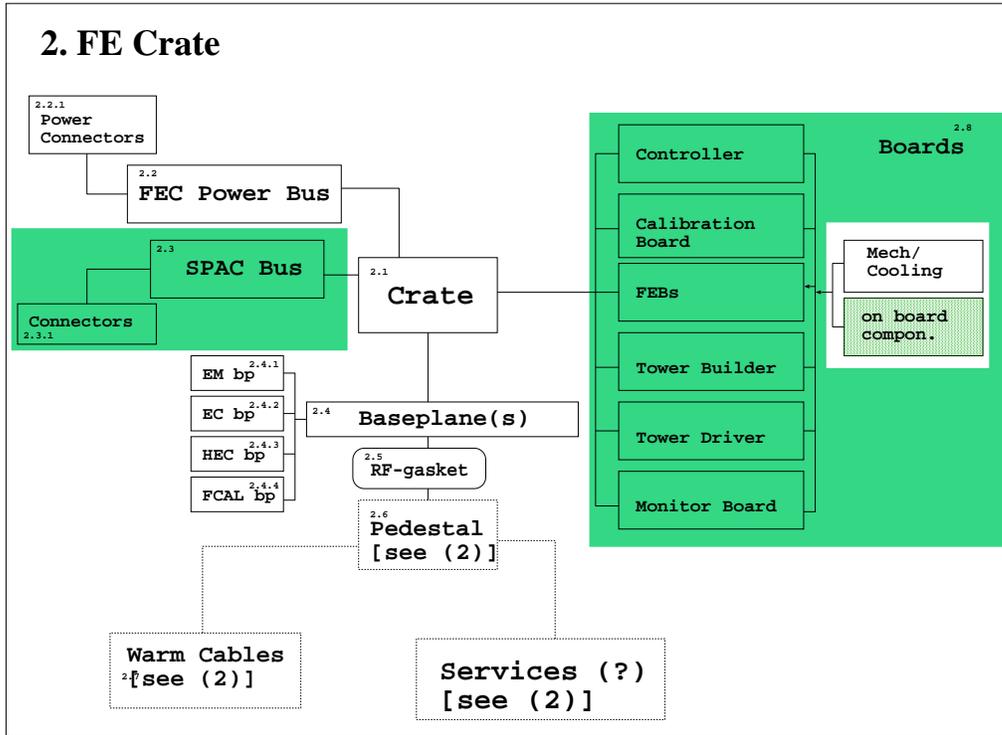


Figure 3: Front-End crate components and block diagram

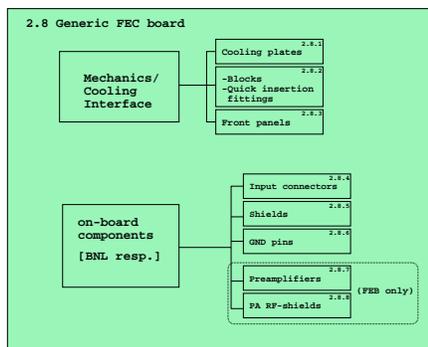


Figure 4: BNL deliverables for board production and assembling

Table 2: FEC status and plan summary table

Component	ID tag	Status/Plan	Completion date
Crate	2.1	ready	-
Power Bus	2.2	installed	-
comb connectors	2.2.1	available	-
SPAC bus	2.3	???	???
spac connectors	2.3.1	???	???
Baseplanes			
barrel bspl.	2.4.1		
EC spec. bspl.	2.4.2		
HEC bspl.	2.4.3	available	-
FCAL bspl.	2.4.4		
RF gasket	2.5	available	-
Pedestal	2.6	installed	-
Warm cables	2.7	available	-
Boards	2.8		
Cooling plates	2.8.1	design to be finalized	
		Plate Design (hole pattern)	Feb. 02 (??)
		Production	beg. of Apr 02
		Short version test	mid April
		ready for installation	Jun 02
Blocks+fittings	2.8.2	to be manufactured in house	
		I/O Intfc: prototype ready	Jul 02
		Contacts design	1 week after delivery
		production	+ 1 week
Front Panels	2.8.3	design to be finalized	3rd week of July
Input Connectors	2.8.4	on order	end of Feb.
Shields	2.8.5	on order	end of Feb.
GND pins	2.8.6	available	-
Preamplifiers (FEB only)	2.8.7	available	-
PA RF-shields (FEB only)	2.8.8	on order	end of Feb.
Hypertronics power conn	2.8.9	available	-
TTC cabling	2.9	???	???

3 Input load and services

One of the goal of the crate-tests is to determine how the system limits the performances of the front-end boards in terms of coherent noise. The load at the input affects in a significant manner the coherent noise level as established by independent measurements. Also testbeam data seems to show that coherent noise is almost factor 2 higher than what specified in the TDR. It's our belief that the task-force should address the problem with the highest priority.

Furthermore, the tower-builder and the calibration board tests will presumably require the possibility to inject signals at the level of the motherboard We assume here that: i) we will have all the warm cables. ii) we will have 2 vacuum FTs available.

Several scenarios can be foreseen for loading the preamplifier inputs.

1. a simplest solution would be to prepare small patch cards (with capacitive loads) to be installed right at the baseplane inputs or equivalently at the level of the pigtailed. While this option is particular restrictive can be usefull in the early stages of the tests to debug/understand the system and the noise properties
2. an hybrid solution where the N boards to be readout for the crate-tests are equipped with toy calorimeters (which imply motherboard/summing board and cold cables) while the remaining ones with the patch cards discussed previously
3. a full toy-calorimeter solution where all the 28 boards are loaded with FTs + cold cables + MB + SB + toy calorimeters (see Fig. 5).

Clearly either option 2. or 3. are the only ones that guarantee a setup close to the real one, in particular for what concern grounding. On the other end possible problems are costs of the parts and the availability of parts like the cold cables. Table 3 (still in preparation) summarizes the status of the input loads and of the services that we propose to have on the setup

Table 3: summary of the possible input load/services for the crate-tests

Item	ID Tag	Status	Availability
Pedestal	3.1	installed	-
Warm cables	3.2	available	-
FT	3.3	in production	April 2002
Patch panel	3.4	needed (??)	??
Cold cables	3.5	??	??
Input loads	3.6		
Motherboards	3.6.1	??	??
Summing Boards	3.6.2	??	??
Toy calorimeters	3.6.3	3 available	??
Patch cards	3.6.4	cost estimate	??
Services	3.7		
pedestal svc.	3.7.1	to be installed	end Mar 2002
Filter box	3.7.2	in construction	end Mar 2002 (??)

4 Power Supply

Fig. 6 depicts a diagram of the scheme we propose to use for the power supply system. Items 4.1 and 4.2 are concerning the laboratory infrastructures and not directly the the crate tests.

The plan is to use an high voltage (operated between 200 and 300V) PS through an insulated transformer. Such a power unit has not been decided yet.

The DC-DC converter 4.6 will be a Modular Devices Inc. prototype that will be ready by the beginning of July. Still the definition of the sense lines and the interface to the monitor system has not been defined yet. Table 4 summarizes the status and the plans for the power supply:

Table 4: Power Supply system status and plan summary table

Component	ID tag	Status/Plan	Completion date
200-300V PS unit	4.4	to be determined	
200-300V cables	4.5	to be determined	
MDI LV module Design Production Installation	4.6	mechanical layout to be completed (2 prototypes) ready for installation by	Feb. 02 end of July 02 08/01/02
connectors	4.7	available	
PS2FEC cables	4.8	not defined yet	

5 Monitor and interlock system

Monitor and interlock is in our opinion extremely critical during the crate-tests operations. We have to plan in advance that the site housing the crate-tests keeps the operation 24h a day for a long period (≥ 4 months). Unfortunately nothing is basically existing, parameters to monitor online and to form the interlock logic have yet to be completely defined. The design has to finalized in the next couple of months and realized by the beginning of the summer if we want the tests to really start in the fall. Fig. 7 depicts a possible scenario for a system monitoring the crate and the power supply parameters for an interlock inputs that we just started thinking in BNL.

6 Cooling

The existing cooling system (its block diagram is depicted in Fig. 8) is very likely adequate for running the crate-tests. Only few issues have been left open and are here summarized:

- Manifolds will have to be replaced once the final insertion fitting will be decided (see table 1)
- Extensive tests have to be done at full load to understand the efficiency and the stability of the system on a long time-scale. Dummy loads (already existing) will be used for such tests
- The current system use a proprietary monitor/control software that is not compatible with the Atlas DCS. An interface to the interlock circuitry has to be designed (see Sec. 5).

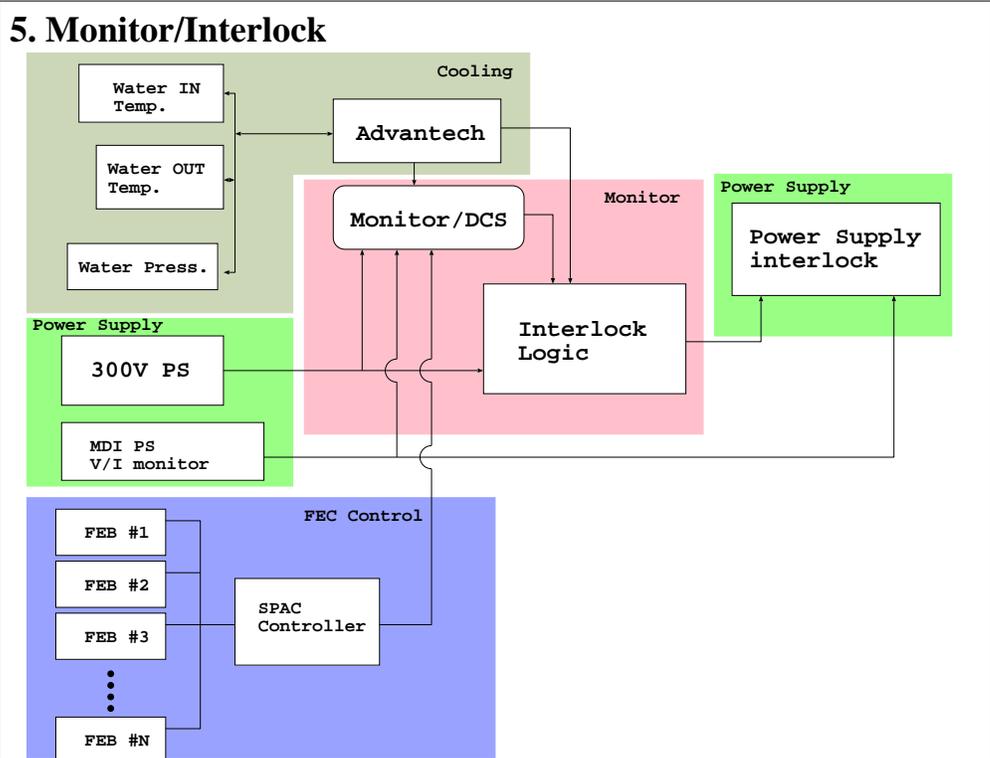


Figure 7: A possible scenario for monitor/interlock system at a crate test

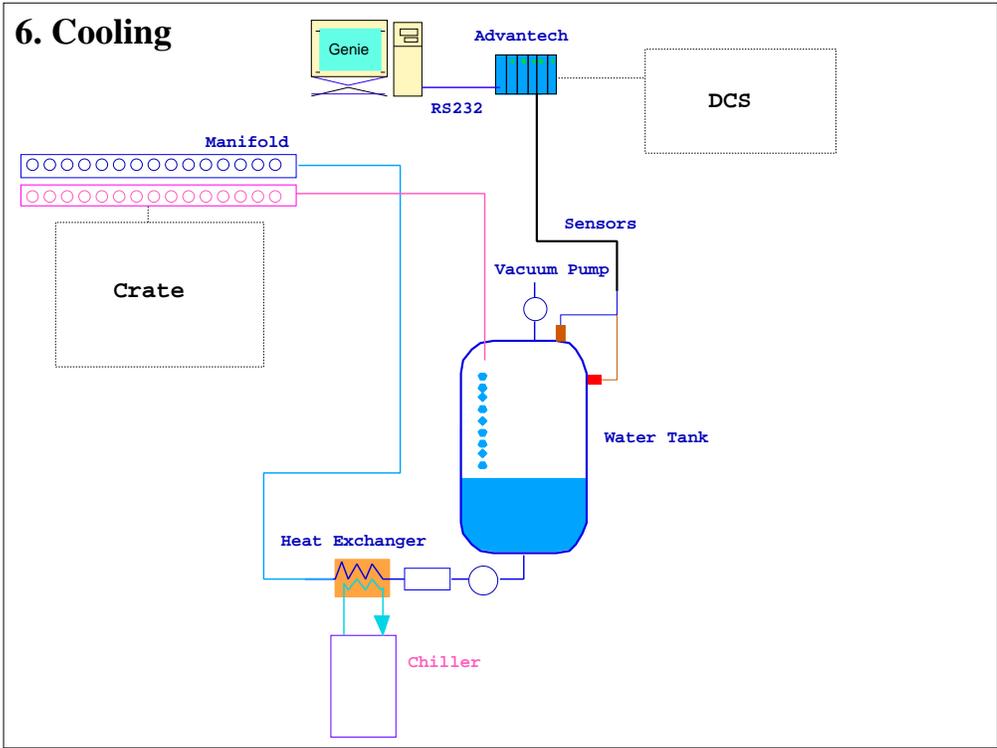


Figure 8: Current cooling system used in the BNL mockup

7 L1 system

Analog sums are needed in the crate-tests at least for two purposes: i) system validation of the tower builder/driver boards and ii) complementary informations that can be obtained for noise studies. A minimum "L1 system" is needed: this has to include of course a receiver and an ADC. The problem of correlating event by event data from the analog sums and from the ROD-like DAQ system has yet to be addressed.

8 DAQ system

The DAQ system we are proposing is schematically depicted in Fig. 1.

- **A Linux box** acts as user interface, data storage and control/DAQ station through the ATLAS/DAQ-1 framework.
- **A VME/PCI bridge** by Bit3 Inc. accesses a VME crate where the SPAC master, the TTC control and a PTG (= programmable trigger generator) that we have built last year for driving an external waveform generator and simulating physics signals in the toy calorimeters).
- **A single CPU board in a VME64 crate** (Host 2 in Fig. 9) downloads the code into the DSPs and accesses the RODs (or better the Nevis boards John mentioned) data and transfer them through the VME bus and a 100Mbit ethernet switch to the linux box.

A possible dataflow of the data is shown in Fig. 9 Some expertise have been developed in situ with the ATLAS/DAQ-1 software. For obvious reasons we propose to continue with that software. Of course more integration and new code is needed since most of the hardware is likely to be changed but the whole process should fit well in the time-schedule foreseen for the tests.

TODO

1. **SPAC master.** In the current setup a SPAC master sitting on the control VME crate is directly linked to the crate boards. In the new configuration there will be a point-to-point link to the crate controller. We need to know what hardware is required and how the communication is established,
2. **TTC control** We contacted Per Gallno at CERN to have TTC/vx and TTC/vi boards here. BNL intends to buy them for a permanent installation in the setup. Such boards are going to be manufactured now and will not be available before June. However a limited preproduction series will be presumably available earlier. Unfortunately there is already a long queue, we need help from the electronic conveners to be prioritized (Philippe Fartouat is the contact for LARG).
3. **DAQ Software** we are going to upgrade the system. It will require 3/4weeks (with some safety margin included). Clearly the communication software to the crate boards will be an issue by the time such boards will be available. Therefore it's important for all the institutions participating in the effort to share the informations as much as possible and enough in advance.

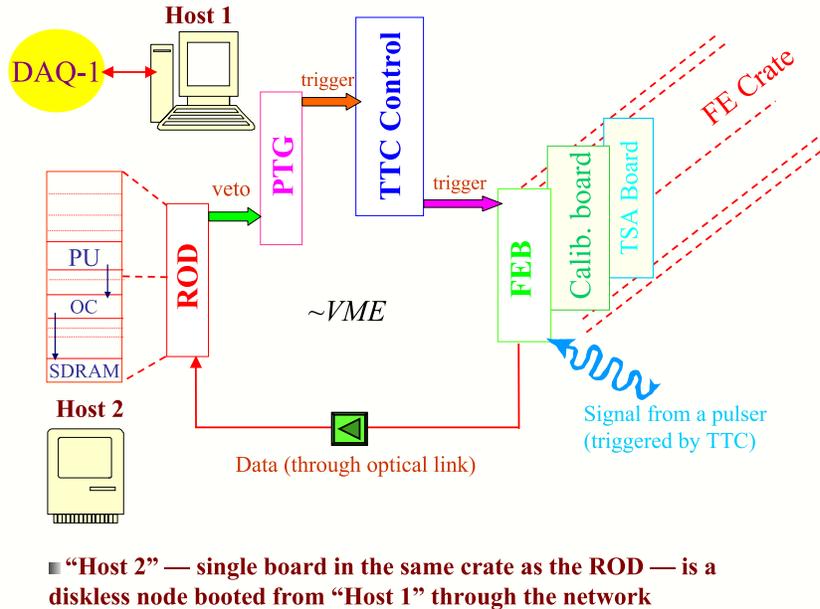


Figure 9: FEB/ROD dataflow in the DAQ system currently run at BNL

Manpower

The crate-tests are meant to be an effort of the full LARG community. Contribution and collaboration by everyone is mandatory for determining the success of such tests. On the other end it's clear that the site hosting the tests should have the responsibility to coordinate the operations and the organization of the tests.

For what concern the people in BNL who can contribute a list is following, each with his expertise or field of interest: some of them (1,4,5,7) can actually be available for a large fraction of their time to the development and the operations while for the remaining the contribution will be limited by the responsibilities they have in other activities.

1. F. Lanni
2. H. Takai - crate system, power supply
3. S. Rescia - grounding, noise...
4. M. Leite - mockup, input loads, lab infrastructures
5. H. Cheng - slow control, monitor, trigger/timing
6. J. Kierstead - power supply
7. K. Yip - ROD interface, DAQ
8. D. Makowiecki - Filter Box
9. B. Hackenburg - FT and services

The proximity of other labs/universities and in particular of Nevis (FEBs,RODs) and Stony Brook (RODs) is also very important and BNL should expect to work closely with them.